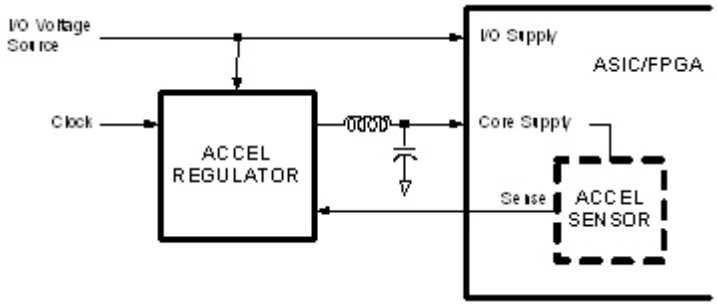
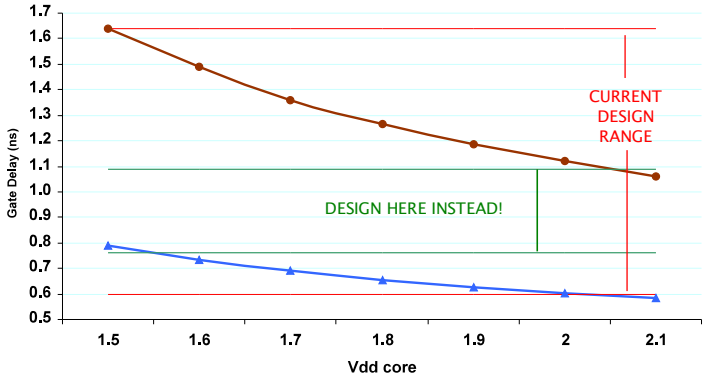
Accel (Patent Pending) INNOTECH SYSTEMS, INC.

Our unique product automatically controls the supply voltage to your ASIC or FPGA to optimize performance!

- ✔ Speed increase: 45% in 0.13um, 35% in 0.18um
- ✔ Power savings: 40% in 0.13um, 35% in 0.18um
- ✔ Get next generation speeds from your current process
  - ▸ much lower mask and die costs
  - ▸ lower design risk
  - ▸ better IP availability
- ✔ Simpler timing closure leads to rapid product development
- ✔ Accel may be entirely enclosed in your ASIC package
  - ▸ reduce package pin count
  - ▸ single supply finished product
- ✔ Extends product life
- ✔ Applicable to any sub-0.35um CMOS technology

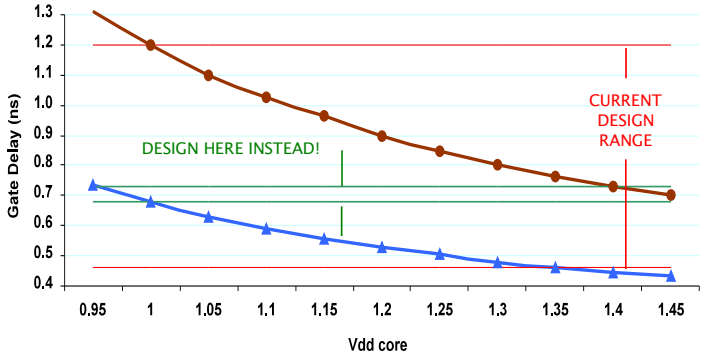


TSMC 0.18µm Technology Timing Delays



0.18µm design conditions example:	Design limit:	with Accel-SP:
Speed: SS, 125C, 1.8v - 10% - 100mV	150 MHz	→ 205 MHz
Power: FF, 0C, 1.8v +10%	1.00 W	→ 0.62 W

TSMC 0.13µm Technology Timing Delays



0.13µm design conditions example:	Design limit:	with Accel-SP:
Speed: SS, 125C, 1.2v - 10% - 80mV	200 MHz	→ 290 MHz
Power: FF, 0C, 1.2v +10%	1.00 W	→ 0.59 W

Get better speed and power specs from your ASIC's! Accel adjusts and regulates your design's core supply based on a reference clock signal and sensor information received from the on-chip IP block. The generated voltage is tailored specifically to the design's process and operating conditions to continuously optimize performance. Accel incorporates a buck regulator for high conversion efficiency. Your product performance will be much more consistent even with large processing variations and yields can be improved.

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